

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

(original)

1. / A method for testing faults propagated to the data ports and asynchronous set/reset

5        ports of selected scan cells in a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of set/reset circuitries, a plurality of set/reset controllers, and a plurality of scan chains, each scan chain comprising multiple scan cells coupled in series, each scan cell having one or more clocks and each set/reset controller having a scan enable (SE)

10       signal and a set/reset enable (SR\_EN) signal; said method comprising:

(a) shifting in a stimulus to all said scan cells in said scan-based integrated circuit by enabling all said scan enable (SE) signals connected to all said scan cells during a shift-in operation;

15       (b) capturing a test response of all said scan cells for testing said faults propagated to said data ports and said asynchronous set/reset ports of all said selected scan cells by enabling or disabling all said set/reset enable (SR\_EN) signals connected to all said selected scan cells during a capture operation;

20       (c) shifting out said test response for comparison or compaction while shifting in a new stimulus to all said scan cells during a shift-out operation

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(d) ; and

(e) repeating steps (b) to (c) until a limiting criteria is reached.

(original)

2. /The method of claim 1, wherein said shifting in a stimulus to all said scan cells further comprises selectively shifting in a predetermined stimulus from an ATE (automatic test equipment) in said selected scan-test mode or shifting in a pseudo-random stimulus automatically generated in said scan-based integrated circuit using a pseudo-random pattern generator (PRPG) in said selected self-test mode during said shift-in operation.

(original)

3. /The method of claim 1, wherein said shifting in a stimulus to all said scan cells further comprises using all said set/reset enable (SR\_EN) signals to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in operation.

(original)

4. /The method of claim 1, wherein said capturing a test response of all said scan cells further comprises selectively disabling all said scan enable (SE) signals simultaneously or in an ordered sequence during said capture operation.

(original)

5. /The method of claim 1, wherein said capturing a test response of all said scan cells further comprises disabling all said clocks controlling all said scan cells, while enabling all said set/reset enable (SR\_EN) signals, for testing said faults propagated to said asynchronous set/reset ports of all said selected scan cells during said capture operation.

(original)

6. /The method of claim 5, wherein said enabling all said set/reset enable (SR\_EN) signals further comprises selectively enabling two or more said set/reset enable (SR\_EN) signals simultaneously or in an ordered sequence during said capture operation.

(original)

7. /The method of claim 1, wherein said capturing a test response of all said scan cells further comprises enabling all said clocks controlling all said scan cells, while disabling all said set/reset enable (SR\_EN) signals, for testing said faults propagated to said data ports of all said selected scan cells during said capture operation.

(original)

8. /The method of claim 7, wherein said enabling all said clocks controlling all said scan cells further comprises selectively enabling two or more said clocks controlling two or more said scan cells simultaneously or in an ordered sequence during said capture operation.

9. (currently amended) The method of claim [[1]] 2, wherein said shifting out said test response for comparison or compaction further comprises selectively shifting out said test response to said ATE for comparison in said selected scan-test mode or shifting out said test response for compaction using a compactor, including a multiple-input signature register (MISR), in said selected self-test mode during said shift-out operation.

(original)

10/ The method of claim 1, wherein said set/reset controller further comprises providing a shift controller and a capture controller in response to a said scan enable (SE) signal and a said set/reset enable (SR\_EN) signal, wherein said shift controller is adapted to disable said asynchronous set/reset ports of one or more said selected scan cells during said shift-in or said shift-out operation, and wherein said capture controller is adapted to enable or disable propagation of said faults present in one said set/reset circuitry to said asynchronous set/reset ports of one or more said selected scan cells during said capture operation.

(original)

11/ The method of claim 1, wherein said scan enable (SE) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)

12/ The method of claim 11, wherein all said scan enable (SE) signals are further driven by one or more global scan enable (global\_SE) signals, wherein each said global scan enable (global\_SE) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)

13/ The method of claim 1, wherein said set/reset enable (SR\_EN) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)

14./The method of claim 13, wherein all set/reset enable (SR\_EN) signals are further driven by one or more global set/reset enable (global\_SR\_EN) signals, wherein each said global set/reset enable (global\_SR\_EN) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)

15./The method of claim 1, wherein said scan cell is a multiplexed-type D flip-flop, a two-port D flip-flop, or a LSSD (level-sensitive scan design) SRL (shift register latch).

(original)

16./The method of claim 1, wherein said set/reset controller is used to repair one or more asynchronous set/reset violations, comprising sequentially-gated set/reset violations, combinational-gated set/reset violations, generated set/reset violations, and destructive set/reset violations, in a selected set/reset circuitry in said scan-based integrated circuit.

(original)

17./A set/reset controller having a scan enable (SE) signal and a set/reset enable (SR\_EN) signal for testing faults propagated to the data ports and asynchronous set/reset ports of selected scan cells in a scan-based integrated circuit, the scan-based integrated circuit containing a plurality of set/reset circuitries and a plurality of scan chains, each scan chain comprising multiple scan cells coupled in series, each scan cell having one or more clocks; said set/reset controller comprising:

(a) a shift controller, inserted between a selected set/reset circuitry and said asynchronous set/reset ports of all said selected scan cells, for disabling said asynchronous set/reset ports of all said selected scan cells, in response to said scan enable (SE) signal and said set/reset enable (SR\_EN) signal, during a shift-in or shift-out operation; and

(b) a capture controller, inserted between said selected set/reset circuitry and said asynchronous set/reset ports of all said selected scan cells, for enabling or disabling propagation of said faults present in said selected set/reset circuitry to said asynchronous set/reset ports of all said selected scan cells, in response to said scan enable (SE) signal and said set/reset enable (SR\_EN) signal, during a capture operation.

(currently amended)

18. The set/reset controller of claim 17, wherein said shift controller is selectively embedded in said selected set/reset circuitry or in all said selected scan cells, and wherein said scan enable (SE) signal, said set/reset enable (SR\_EN) signal, or said scan enable (SE) signal and said set/reset enable (SR\_EN) signal can be selectively used to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or shift-out operation.

(original)

19. The set/reset controller of claim 17, wherein said capture controller further comprises selectively disabling all said scan enable (SE) signals simultaneously or in an ordered sequence during said capture operation.

(original)

20. The set/reset controller of claim 17, wherein said capture controller further comprises disabling all said clocks controlling all said scan cells, while enabling all said set/reset enable (SR\_EN) signals, for testing said faults propagated to said asynchronous set/reset ports of all said selected scan cells during said capture operation.

(original)

21. The set/reset controller of claim 20, wherein said enabling all said set/reset enable (SR\_EN) signals further comprises selectively enabling two or more said set/reset enable (SR\_EN) signals simultaneously or in an ordered sequence during said capture operation.

(original)

22. The set/reset controller of claim 17, wherein said capture controller further comprises enabling all said clocks controlling all said scan cells, while disabling all said set/reset enable (SR\_EN) signals, for testing said faults propagated to said data ports of all said selected scan cells during said capture operation.

(original)

23. The set/reset controller of claim 22, wherein said enabling all said clocks controlling all said scan cells further comprises selectively enabling two or more said clocks

controlling two or more said scan cells simultaneously or in an ordered sequence during said capture operation.

(original)

24. The set/reset controller of claim 17, wherein said capture controller is selectively embedded in said selected set/reset circuitry or in all said selected scan cells.

(original)

25. The set/reset controller of claim 17, wherein said scan enable (SE) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)

26. The set/reset controller of claim 25, wherein all said scan enable (SE) signals are further driven by one or more global scan enable (global\_SE) signals, wherein each said global scan enable (global\_SE) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)

27. The set/reset controller of claim 17, wherein said set/reset enable (SR\_EN) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)

28. The set/reset controller of claim 27, wherein all set/reset enable (SR\_EN) signals are further driven by one or more global set/reset enable (global\_SR\_EN) signals, wherein

each said global set/reset enable (global\_SR\_EN) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)

29. The set/reset controller of claim 17, wherein said scan cell is a multiplexed-type D flip-flop, a two-port D flip-flop, or a LSSD (level-sensitive scan design) SRL (shift register latch).

(original)

30. The set/reset controller of claim 17, wherein said shift controller and capture controller are used to repair one or more asynchronous set/reset violations, comprising sequentially-gated set/reset violations, combinational-gated set/reset violations, generated set/reset violations, and destructive set/reset violations, in said selected set/reset circuitry in said scan-based integrated circuit.

(original)

31. A method for synthesizing a plurality of set/reset controllers each having a scan enable (SE) signal and a set/reset enable (SR\_EN) signal for testing faults propagated to the data ports and asynchronous set/reset ports of selected scan cells in a scan-based integrated circuit, the scan-based integrated circuit containing a plurality of set/reset circuitries and a plurality of scan chains, each scan chain comprising multiple scan cells coupled in series, each scan cell having one or more clocks; said method comprising the computer-implemented steps of:

- (a) compiling the HDL (hardware description language) code modeled at RTL (register-transfer level) or gate-level that represents said scan-based integrated circuit into a sequential circuit model;
- (b) specifying a list of asynchronous set/reset signals each causing one or more asynchronous set/reset violations in each selected set/reset circuitry for repair;
- (c) synthesizing a said plurality of set/reset controllers, each having a said scan enable (SE) signal and a said set/reset enable (SR\_EN) signal, on said sequential circuit model according to said list of asynchronous set/reset signals; and
- (d) generating the repaired HDL code in a selected RTL or gate-level format.

(original)

32/ The method of claim 32, wherein said specifying a list of asynchronous set/reset signals further comprises automatically identifying said list of asynchronous set/reset signals using simulation methods.

(original)

33/ The method of claim 32, wherein said set/reset controller in said synthesizing a said plurality of set/reset controllers further comprises

- (e) a shift controller, inserted between said selected set/reset circuitry and said asynchronous set/reset ports of all said selected scan cells, for disabling said

asynchronous set/reset ports of all said selected scan cells, in response to said scan enable (SE) signal and said set/reset enable (SR\_EN) signal, during a shift-in or shift-out operation; and

- (f) a capture controller, inserted between said selected set/reset circuitry and said asynchronous set/reset ports of all said selected scan cells, for enabling or disabling propagation of said faults present in said selected set/reset circuitry to said asynchronous set/reset ports of one or more said selected scan cells, in response to said scan enable (SE) signal and said set/reset enable (SR\_EN) signal, during a capture operation.

(original)

- 34. The method of claim 33, wherein said shift controller is selectively embedded in said selected set/reset circuitry or in one or more said selected scan cells, and wherein said enable (SE) signal, said set/reset enable (SR\_EN) signal, or said scan enable (SE) signal and said set/reset enable (SR\_EN) signal can be selectively used to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or said shift-out operation.

(original)

- 35. The method of claim 33, wherein said capture controller further comprises selectively disabling all said scan enable (SE) signals simultaneously or in an ordered sequence during said capture operation.

(original)

36/ The method of claim 33, wherein said capture controller further comprises disabling all said clocks controlling all said scan cells, while enabling all said set/reset enable (SR\_EN) signals, for testing said faults propagated to said asynchronous set/reset ports of one or more said selected scan cells during said capture operation.

(original)

37/ The method of claim 36, wherein said enabling all said set/reset enable (SR\_EN) signals further comprises selectively enabling two or more said set/reset enable (SR\_EN) signals simultaneously or in an ordered sequence during said capture operation.

(original)

38/ The method of claim 33, wherein said capture controller further comprises enabling all said clocks controlling all said scan cells, while disabling all said set/reset enable (SR\_EN) signals, for testing said faults propagated to said data ports of all said selected scan cells during said capture operation.

(original)

39/ The method of claim 38, wherein said enabling all said clocks controlling all said scan cells further comprises selectively enabling two or more said clocks controlling two or more said selected scan cells simultaneously or in an ordered sequence during said capture operation.

(original)

40/ The method of claim 33, wherein said capture controller is selectively embedded in said selected set/reset circuitry or in said selected scan cells.

(original)  
41/ The method of claim 33, wherein said scan enable (SE) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)  
42/ The method of claim 41, wherein all said scan enable (SE) signals are further driven by one or more global scan enable (global\_SE) signals, wherein each said global scan enable (global\_SE) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)  
43/ The method of claim 33, wherein said set/reset enable (SR\_EN) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)  
44/ The method of claim 43, wherein all set/reset enable (SR\_EN) signals are further driven by one or more global set/reset enable (global\_SR\_EN) signals, wherein each said global set/reset enable (global\_SR\_EN) signal is selectively generated in said scan-based integrated circuit or an input signal to said scan-based integrated circuit.

(original)  
45/ The method of claim 33, wherein said scan cell is a multiplexed-type D flip-flop, a two-port D flip-flop, or a LSSD (level-sensitive scan design) SRL (shift register latch).

(original)

46. The method of claim 33, wherein said shift controller and capture controller are used to repair one or more asynchronous set/reset violations, comprising sequentially-gated set/reset violations, combinational-gated set/reset violations, generated set/reset violations, and destructive set/reset violations, in said selected set/reset circuitry in said scan-based integrated circuit.

(original)

47. A method for generating stimuli and test responses for testing faults propagated to the data ports and asynchronous set/reset ports of selected scan cells in a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of set/reset circuitries, a plurality of set/reset controllers, and a plurality of scan chains, each scan chain comprising multiple scan cells coupled in series, each scan cell having one or more clocks and each set/reset controller having a scan enable (SE) signal and a set/reset enable (SR\_EN) signal; said method comprising the computer-implemented steps of:

(a) compiling the HDL (hardware description language) code modeled at RTL (register-transfer level) or gate-level that represents said scan-based integrated circuit into a sequential circuit model;

(b) specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals during a shift-in, capture, or shift-out operation;

(c) transforming said sequential circuit model into an equivalent combinational circuit model; and

(d) generating said stimuli and said test responses according to said input constraints and said combinational circuit model.

(original)

48./The method of claim 47, wherein said specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said set/reset enable (SR\_EN) signals to logic value 1 to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or said shift-out operation.

(original)

49./The method of claim 47, wherein said specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said scan enable (SE) signals to logic value 1 to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or said shift-out operation.

(original)

50./The method of claim 47, wherein specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises selectively setting all said scan enable (SE) signals to logic value 0 simultaneously or in an ordered sequence during said capture operation.

(original)

51. The method of claim 47, wherein specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said clocks controlling all said scan cells to logic value 0, while setting all said set/reset enable (SR\_EN) signals to logic value 1, for testing said faults propagated to said asynchronous set/reset ports of all said selected scan cells during said capture operation.

(original)

52. The method of claim 51, wherein said setting all said set/reset enable (SR\_EN) signals to logic value 1 further comprises selectively setting two or more said set/reset enable (SR\_EN) signals to logic value 1 simultaneously or in an ordered sequence during said capture operation.

(original)

53. The method of claim 47, wherein specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said clocks controlling all said scan cells to logic value 1, while setting all said set/reset enable (SR\_EN) signals to logic value 0, for testing said faults propagated to said data ports of all said selected scan cells during said capture operation.

(original)

54. The method of claim 53, wherein said setting all said clocks controlling all said scan cells to logic value 1 further comprises selectively setting two or more said clocks

controlling two or more said scan cells to logic value 1 simultaneously or in an ordered sequence during said capture operation.

(original)

55. The method of claim 47, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises performing fault simulation on said combinational circuit model using a selected set of predetermined patterns in said selected scan-test mode or a selected set of pseudo-random patterns in said selected self-test mode.

(original)

56. The method of claim 47, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises performing combinational ATPG (automatic test pattern generation) on said combinational circuit model to generate said stimuli and said test responses in said selected scan-test mode.

(original)

57. The method of claim 47, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises generating HDL test benches according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit using simulation methods.

(original)

58. The method of claim 47, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises generating ATE (automatic test equipment) test programs according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit in said ATE.

(original)

59. A computer-readable memory having computer-readable program code embodied therein for causing a computer system to perform a method for generating stimuli and test responses for testing faults propagated to the data ports and asynchronous set/reset ports of selected scan cells in a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of set/reset circuitries, a plurality of set/reset controllers, and a plurality of scan chains, each scan chain comprising multiple scan cells coupled in series, each scan cell having one or more clocks and each set/reset controller having a scan enable (SE) signal and a set/reset enable (SR\_EN) signal; said method comprising the computer-implemented steps of:

(a) compiling the HDL (hardware description language) code modeled at RTL (register-transfer level) or gate-level that represents said scan-based integrated circuit into a sequential circuit model;

(b) specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals during a shift-in, capture, or shift-out operation;

(c) transforming said sequential circuit model into an equivalent combinational circuit model; and

(d) generating said stimuli and said test responses according to said input constraints and said combinational circuit model.

(original)

60. The computer-readable memory of claim 59, wherein said specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said set/reset enable (SR\_EN) signals to logic value 1 to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or said shift-out operation.

(original)

61. The computer-readable memory of claim 59, wherein said specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said scan enable (SE) signals to logic value 1 to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or said shift-out operation.

(original)

62. The computer-readable memory of claim 59, wherein specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises selectively setting all said scan enable (SE) signals to logic value 0 simultaneously or in an ordered sequence during said capture operation.

(original)

63. The computer-readable memory of claim 59, wherein specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said clocks controlling all said scan cells to logic value 0, while setting all said set/reset enable (SR\_EN) signals to logic value 1, for testing said faults propagated to said asynchronous set/reset ports of all said selected scan cells during said capture operation.

(original)

64. The computer-readable memory of claim 63, wherein said setting all said set/reset enable (SR\_EN) signals to logic value 1 further comprises selectively setting two or more said set/reset enable (SR\_EN) signals to logic value 1 simultaneously or in an ordered sequence during said capture operation.

(original)

65. The computer-readable memory of claim 59, wherein specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said clocks controlling all said scan cells to logic value 1, while setting all said set/reset enable (SR\_EN) signals to logic value 0, for testing said

faults propagated to said data ports of all said selected scan cells during said capture operation.

(original)

66./The computer-readable memory of claim 65, wherein said setting all said clocks controlling all said scan cells to logic value 1 further comprises selectively setting two or more said clocks controlling two or more said scan cells to logic value 1 simultaneously or in an ordered sequence during said capture operation.

(original)

67./The computer-readable memory of claim 59, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises performing fault simulation on said combinational circuit model using a selected set of predetermined patterns in said selected scan-test mode or a selected set of pseudo-random patterns in said selected self-test mode.

(original)

68./The computer-readable memory of claim 59, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises performing combinational ATPG (automatic test pattern generation) on said combinational circuit model to generate said stimuli and said test responses in said selected scan-test mode.

(original)

69./The computer-readable memory of claim 59, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit

model further comprises generating HDL test benches according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit using simulation methods.

(original)

70. The computer-readable memory of claim 59, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises generating ATE (automatic test equipment) test programs according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit in said ATE.

(original)

71. An electronic design automation system comprising: a processor; a bus coupled to said processor, and a computer-readable memory coupled to said bus and having computer-readable program code stored therein for causing said electronic design automation system to perform a method for generating stimuli and test responses for testing faults propagated to the data ports and asynchronous set/reset ports of selected scan cells in a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of set/reset circuitries, a plurality of set/reset controllers, and a plurality of scan chains, each scan chain comprising multiple scan cells coupled in series, each scan cell having one or more clocks and each set/reset controller having a scan enable (SE) signal and a set/reset enable (SR\_EN) signal; said method comprising the computer-implemented steps of:

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- (a) compiling the HDL (hardware description language) code modeled at RTL (register-transfer level) or gate-level that represents said scan-based integrated circuit into a sequential circuit model;
- (b) specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals during a shift-in, capture, or shift-out operation;
- (c) transforming said sequential circuit model into an equivalent combinational circuit model; and
- (d) generating said stimuli and said test responses according to said input constraints and said combinational circuit model.

(original)

72. The system of claim 71, wherein said specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said set/reset enable (SR\_EN) signals to logic value 1 to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or said shift-out operation.

(original)

73. The system of claim 71, wherein said specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises

setting all said scan enable (SE) signals to logic value 1 to disable all said asynchronous set/reset ports of all said selected scan cells during said shift-in or said shift-out operation.

(original)

74. The system of claim 71, wherein specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises selectively setting all said scan enable (SE) signals to logic value 0 simultaneously or in an ordered sequence during said capture operation.

(original)

75. The system of claim 71, wherein specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said clocks controlling all said scan cells to logic value 0, while setting all said set/reset enable (SR\_EN) signals to logic value 1, for testing said faults propagated to said asynchronous set/reset ports of all said selected scan cells during said capture operation.

(original)

76. The system of claim 75, wherein said setting all said set/reset enable (SR\_EN) signals to logic value 1 further comprises selectively setting two or more said set/reset enable (SR\_EN) signals to logic value 1 simultaneously or in an ordered sequence during said capture operation.

(original)

77. The system of claim 71, wherein specifying input constraints on said clocks, said scan enable (SE) signals, and said set/reset enable (SR\_EN) signals further comprises setting all said clocks controlling all said scan cells to logic value 1, while setting all said set/reset enable (SR\_EN) signals to logic value 0, for testing said faults propagated to said data ports of all said selected scan cells during said capture operation.

(original)

78. The system of claim 77, wherein said setting all said clocks controlling all said scan cells to logic value 1 further comprises selectively setting two or more said clocks controlling two or more said scan cells to logic value 1 simultaneously or in an ordered sequence during said capture operation.

(original)

79. The system of claim 71, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises performing fault simulation on said combinational circuit model using a selected set of predetermined patterns in said selected scan-test mode or a selected set of pseudo-random patterns in said selected self-test mode.

(original)

80. The system of claim 71, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises performing combinational ATPG (automatic test pattern generation) on said

combinational circuit model to generate said stimuli and said test responses in said selected scan-test mode.

(original)  
81/The system of claim 71, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises generating HDL test benches according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit using simulation methods.

(original)  
82/The system of claim 71, wherein said generating said stimuli and said test responses according to said input constraints and said combinational circuit model further comprises generating ATE (automatic test equipment) test programs according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit in said ATE.